IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Erik E. Erlandson and David A. Tremblay, Jr.
Title:	MEMORY HAVING INCREASED DATA-TRANSFER SPEED AND RELATED SYSTEMS AND METHODS
Serial Number:	10/032,109
Filing Date:	December 20, 2001
Examiner/Unit:	Jasmine Song/2188
Attorney Docket No.:	10016854-1 (1964-1-3)

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited in the United States Postal Service as First Class mail in an envelope addressed to: MS AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14th day of January, 2005.

Signature

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES PURSUANT TO 37 C.F.R. § 1.131 TO OVERCOME A CITED U.S. PATENT APPLICATION PUBLICATION

TO THE COMMISSIONER FOR PATENTS:

This Declaration establishes completion of the claimed invention in the United States on a date before November 02, 2001, which is the effective date (U.S. filing date) of U.S. Patent Application Publication No. 2002/0110037 to Fukuyama.

We, Erik Erlandson and David Tremblay, Jr. hereby declare the following:

1) We are the inventors of the invention described and claimed in U.S. Patent Application Serial No. 10/032,109, which was filed on December 20, 2001. In the United States, before November 02, 2001, we had conceived of a memory, an electronic system including the memory, and a method for transferring data. Specifically, we had conceived of a memory having the features of claim 1 both as originally filed and as amended prior to and concurrent with the filing of this Declaration. The memory, which we had conceived of before November 02, 2001, included an address bus operable to receive an external address during a data-transfer cycle, an address counter operable to generate an internal address during the data-transfer cycle, an address decoder, a comparator operable to compare the external address to a value, and a control circuit operable to terminate the data-transfer cycle based on the relationship between the external address and the value. Likewise, in the United States before November 02, 2001, we had conceived of a memory as recited in claim 11 both as originally filed and as amended, a memory as recited in claim 38 as originally presented, an electronic system as recited in claim 18 as originally filed, an electronic system as recited in claim 20 both as originally filed and as amended, methods as recited in claims 23, 27, and 34 as originally filed and as amended, a memory as recited in new claim 39 as filed concurrently with this Declaration, and an electronic system as recited in new claim 40 as filed concurrently with this Declaration.

2) From May 17, 2001 through December 20, 2001, we were diligent in constructively reducing the conceived memory, electronic system, and method to practice by filing the present patent application. On May 17, 2001, we submitted to our corporate patent department according to normal corporate procedures an invention disclosure covering the conceived memory, electronic system, and method. On or about June 11, 2001, we understand that our corporate patent department sent our invention disclosure to our patent attorney. On July 13, 2001, at our patent attorney's request, we provided our patent attorney background information and additional drawings showing our invention. On August 7, 2001, we

explained our invention to our patent attorney over the phone. On October 19, 2001, our patent attorney sent us a first draft of the patent application for our review. Within the next few weeks we reviewed the first draft, and on October 31, 2001 we provided our comments to our patent attorney. On November 06, 2001, our patent attorney sent us a final draft of the application, along with a Declaration and Power of Attorney. During the next month, we reviewed and approved the final draft and executed the Declaration and Power of Attorney. On our about December 9, 2001, we sent the approved draft and executed Declaration to our patent attorney, who received the approved draft and Declaration on December 12, 2001. Our attorney then filed the approved application and Declaration on December 20, 2001, which was merely two months after we received the first draft of the application.

3) Exhibit A is a page of an invention disclosure that we submitted to our superiors before November 02, 2001 according to standard corporate procedures. Exhibit A is a timing diagram that that is similar to the timing diagram shown in FIG. 3 (Exhibit B) of the patent application, and, like FIG. 3, shows the generation of a column address by a column-address anticipation counter disposed inside of a memory.

4) Exhibit C is a document that we and our patent attorney developed before November 02, 2001 while our patent attorney was in the process of learning our invention in preparation of drafting the present patent application. Exhibit C is a block diagram that is similar to the diagram shown in FIG. 4 (Exhibit D) of the patent application, and that, like FIG. 4, shows a column-address anticipation counter and circuitry (*e.g.*, multiplexer, comparator, and page-length counter) for determining when to end a data-transfer cycle during which the column-address anticipate counter is active.

5) Exhibits A and C show expressly or inherently each and every element of claim 1 as originally filed and as amended. Specifically, Exhibit C shows an address bus operable to receive an external address (input to the column address buffers) during a data-transfer cycle, an address counter

(column-address-anticipation counter) operable to generate an internal address (a column address) during the data-transfer cycle, an address decoder (column decoder) coupled to the address counter, a comparator (18 in FIG. 4 (Exhibit D)) coupled to the address bus (via the column address buffers) and operable to compare the external address to a value (the output of the column-address-anticipation counter), and a control circuit (24 in FIG. 4 (Exhibit D), inherent in Exhibit C) coupled to the comparator and operable to terminate the data-transfer cycle based on the relationship between the external address and the value.

6) In a similar manner, Exhibits A and C show expressly or inherently each and every element of claim 23 as originally filed and as amended.

7) Exhibits A and C show expressly or inherently each and every element of claim 11 as originally filed and as amended. Specifically, Exhibit C shows a data buffer (column address buffers) operable to receive and hold data during a data-transfer cycle, an address counter (column-address-anticipation counter) operable to generate an internal address (a column address output from the column-address-anticipation counter) during the data-transfer cycle, a programmable storage circuit (page-length counter in Exhibit C, 16 in FIG. 4 (Exhibit D)) operable to store an address value during the data-transfer cycle, a comparator (18 in FIG. 4 (Exhibit D)) coupled to the address counter and the storage circuit and operable to compare the internal address to the address value, and a control circuit (24 in FIG. 4 (Exhibit D), inherent in Exhibit C) coupled to the storage circuit, the comparator, and the data buffer and operable to terminate the data-transfer cycle when the internal address has a predetermined relationship to the address value.

8) In a similar manner, Exhibits A and C show expressly or inherently each and every element of claim 27 as originally filed and as amended, and each and every element of claim 39, which is the same as claim 11 before the amendment made to claim 11 in the response to final office action filed December 20, 2004.

9) Exhibits A and C show expressly or inherently each and every element of claim 18 as originally filed and as amended. Specifically, a data input device (*e.g.*, a keyboard), a data output device (*e.g.*, a display screen), and a computer circuit including processor are inherent in a computer system that incorporates the circuitry of Exhibit C. Furthermore, Exhibit C shows an address bus operable to receive an external address (input to the column address buffers) from the processor during a data transfer between the processor and the memory, an address counter (column-address-anticipation counter) operable to generate an internal address (a column address) during the data transfer, an address decoder (column decoder), and a multiplexer (22 in FIG. 4 (Exhibit D)) coupled to the address bus (via the column address buffers), the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder during the data transfer.

10) Exhibits A and C show expressly or inherently each and every element of claim 20 as originally filed and as amended. Specifically, a data input device (*e.g.*, a keyboard), a data output device (*e.g.*, a display screen), and a computer circuit including processor are inherent in a computer system that incorporates the circuitry of Exhibit C. Furthermore, Exhibit C shows an address counter (column-address-anticipation counter) operable to generate an internal address (a column address output from the column-address-anticipation counter) during a data-transfer cycle between the processor and the memory, a storage circuit (page-length counter in Exhibit C, 16 in FIG. 4 (Exhibit D)) operable to receive and store an address value from the processor before or during the data-transfer cycle, a comparator (18 in FIG. 4 (Exhibit D)) coupled to the address counter and the storage circuit and operable to compare the internal address to the address value, and a control circuit (24 in FIG. 4 (Exhibit D), inherent in Exhibit C) coupled to the storage circuit and the comparator and operable to terminate the data-transfer cycle when the internal address has a predetermined relationship to the address value.

11) In a similar manner, Exhibits A and C show expressly or inherently each and every element of claim 40, which is the same as claim 20 before the amendment made to claim 20 in the response to final office action filed December 20, 2004.

12) Exhibits A and C show expressly or inherently each and every element of claim 34 as originally filed and as amended. Specifically, a memory (the counter in the anticipation burst control logic in Exhibit B, 16 in FIG. 4 (Exhibit D)) is loaded with a count value from an external source, a first address (a column address output from the column-address-anticipation counter) is generated inside of the memory and is distinct from the count value, the count value is incremented or decremented, the count value is compared to a predetermined value (which can be stored in the anticipation burst control logic in Exhibit B, 16 in FIG. 4 (Exhibit D)), and a cycle during which data is being transferred to or from a storage location residing at the first address is terminated if the count value has a predetermined relationship to the predetermined value.

13) Exhibits A and C show expressly or inherently each and every element of claim 38 as originally filed and as amended. Specifically, Exhibit C shows an address bus operable to receive an external address (input to the column address buffers) during a data-transfer cycle, an address counter (column-address-anticipation counter) operable to generate an internal address (a column address) during the data-transfer cycle, an address decoder (column decoder) coupled to the address counter, a comparator (18 in FIG. 4 (Exhibit D)) coupled to the address bus (via the column address buffers) and the address counter and operable to compare the external address to the internal address, and a control circuit (24 in FIG. 4 (Exhibit D), inherent in Exhibit C) coupled to the comparator and operable to enable a data transfer based on the relationship between the external address and the internal address.

14) Per MPEP § 715.09, we are seasonably submitting this Declaration with a supplemental reply after final rejection for the purpose of overcoming a new ground of rejection.

15) We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature — Date

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Page No. Memory System speed enhancer for DRAM & SDRAM

Address lines are multiplexed between Column Address Strobe and Row Address Strobe. To enhance speed of data access, paging mode is used. In page mode, a RAS is asserted FIRST, then a series of CAS go on to access all the columns in that Row. This saves time, as the going back and forth between RAS & CAS has to allow more time for accurate operation.

The present invention would enhance the Page mode operation by anticipating the next Column Address with a synchronous counter internal to the DRAM or SDRAM device. This would allow a page/burst mode which would not have to allow time for Address bus setup and hold to the extent that an unmodified system would.

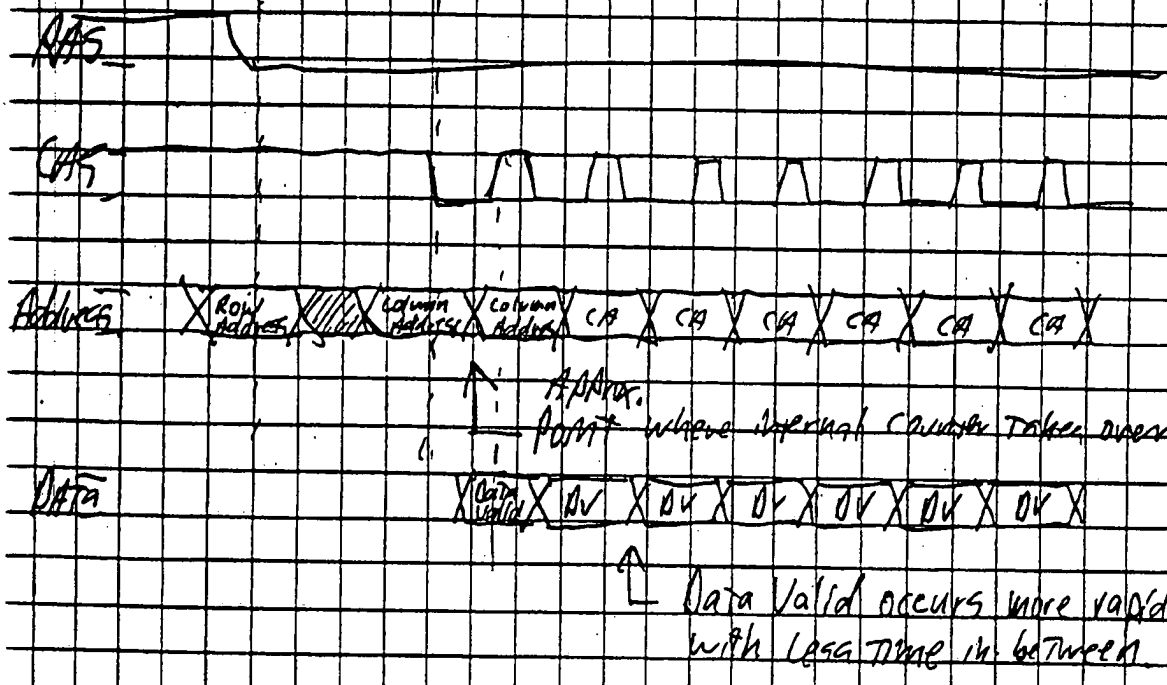

Exhibit A